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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/623,396	07/18/2003	Hing "Thomas" Y. To	42P8816C	4650

8791 7590 11/15/2004

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EXAMINER	
LAU, TUNG S	

ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 11/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/623,396	TO ET AL.	
	Examiner	Art Unit	
	Tung S Lau	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *See office action*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The IDS filed on 7-18-2003 has been accepted and signed by the examiner.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Comino et al. (U.S. Patent 5,914,633).

Regarding claim 1:

Comino discloses a method for current calibration of I/0 cells of an integrated circuit (IC) comprising: setting a global control value provided to the I/O cells; then, for each I/O cell (Col. 4-5, Lines 7-2) comparing the logic voltage at the output pad of the I/0 cell with a reference voltage; sinking more current at the output pad by enabling additional driver bits associated with the I/0 cell if the logic voltage is higher than the reference voltage, or sinking less current at the output pad by disabling additional driver bits associated with the I/O cell if the logic voltage is lower than the reference voltage (Col. 4-5, Lines 7-2, fig. 2a, unit 30, 32, 36).

Regarding claim 6:

Comino discloses a method comprising: setting a global control value provided to the I/O cells, then, for each I/O cell (Col. 4-5, Lines 7-2); setting a local value in a register device associated with the I/O cell in response to the global control value (Col. 4-5, Lines 7-2); comparing the logic voltage at the output pad of the I/O cell with a reference voltage (Col. 4-5, Lines 7-2); sinking more current at the output pad by enabling additional driver bits associated with the I/O cell if the logic voltage is higher than the reference voltage; or sinking less current at the output pad by disabling additional driver bits associated with the I/O cell if the logic voltage is lower than the reference voltage (Col. 4-5, Lines 7-2).

Regarding claim 2, Comino further discloses sinking of more or less current continues until the logic voltage at the pad and the reference voltage are substantially equal (Col. 4-5, Lines 7-2); Regarding claim 3, Comino further discloses enabling/disabling of the additional driver bits is accomplished by modifying a local value stored in a register device associated with the I/O cell depending on the comparison of the logic voltage and the reference voltage (fig. 2a, unit 18, Col. 4-5, Lines 7-2); Regarding claim 4, Comino further discloses shifting 1s or 0s into the register device (fig. 2a, unit 18); Regarding claim 5, Comino further discloses incrementing or decrementing the local value (fig. 2a, unit 18); Regarding claim 7, Comino further discloses modifying the local value in the register device associated with the I/O cell in response to the comparison of

the logic voltage and the reference voltage (Col. 4-5, Lines 7-2); Regarding claim 8, Comino further discloses the disabling of the additional driver bits comprises modifying the local value in the register device associated with the I/0 cell in response to the comparison of the logic voltage and the reference voltage (Col. 4-5, Lines 7-2).

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tung S Lau whose telephone number is 571-272-2274. The examiner can normally be reached on M-F 9-5:30. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on 571-272-2269. The fax phone numbers for the organization where this application or proceeding is assigned is 703-872-9306

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TL
11/12/04

John Barlow
Supervisory Patent Examiner
Technology Center 2800